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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/435,070	11/04/1999	BALARAM SINHAROY	AT9-98-544	4716

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EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/435,070	SINHAROY, BALARAM	
	Examiner	Art Unit	
	William H. Wood	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 1999 and 18 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *2 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Patent Office Communiqué

This detailed action is directed to the acknowledgement of the patent office receiving and beginning an examination of patent application, "Circuits, Systems and Methods for Performing Branch Predictions By Selectively Accessing Bimodal and Fetch-based History Tables" (patent office application number: 09/435,070), being filed on November 4, 1999 and being assigned to Patent Examiner William Wood.

Acknowledgement is made of patent office receiving paper, "Information Disclosure Statement", being filed on December 18, 2000.

Drawings

1. The drawings are objected to because of unclear labeling. It is suggested that the Figures 6 and 7 not include a Figure 6(cont.) and 7(cont.), but instead reference the Figures as 6A-B and 7A-B, similar to what applicant did for Figures 8A and 8B. Should the application for patent be allowed, this will clarify the printing process. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: page 1, lines 4 and 7, are missing application numbers. Appropriate correction is required.

Claim Objections

3. Claim 2 is objected to because of the following informalities: Line 6 of the claim indicates a second value however there is no reference to a first value. It appears that applicant meant to reference a first value in line 4 of the claim. Appropriate correction is required.

4. Claim 19 is objected to because of the following informalities: The word "Clam" to be replaced with "Claim". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 8, 9 and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257.

In regard to claim 1, Patt taught the following limitations:

i) *Branch prediction circuitry* (page 252, title of article)

ii) *a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address* (page 253, section 3.1, item 2 under the bulleted items)

iii) *a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of the*

branch address and bits from a history register (page 253, section 3.1, item 4 under the bulleted items)

iv) *a selector table comprising a plurality of entries each for storing a selection mechanism and accessed by a pointer generated from selected bits from the branch address and bits from the history register* (page 255, section 4, first paragraph and section 4.1, last paragraph; page 255, right column, second paragraph, demonstrates the pointer being generated), *each selector mechanism used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from the fetch-based history table* (page 252, section 2; page 255, section 4.1, first paragraph).

The only limitation, which is not clearly set forth in Patt, is *a selection bit.* However, it is commonly known that for two items, one single bit is all that is required for selecting. This would be more efficient. Therefore, it would have been obvious to one of ordinary skill in the art, to implement the selector table with a selection bit.

In regard to claim 2, the additional limitations *set a corresponding entry in each of the bimodal and fetch-based branch history tables when a branch is taken at branch resolution time* (must record if the branch was taken for the table to be effective) and *set a corresponding entry in each of the bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch time* (must record whether the branch was not taken in order to be effective predicting on the next occurance) are both inherent to branch history tables including the ones found in Patt.

In regard to claim 3, Patt met the additional limitations *update a selected entry in the selector table with a first value when a bimodal prediction value from the bimodal branch history table correctly represents a corresponding branch resolution* (the selector table value for the branches must be updated in accordance with predicting which prediction strategy to go with in order to be effective) and *update a selected entry in the selector table with a second value when a fetch-based prediction value from the fetch-based branch history table correctly represents the corresponding branch resolution* (the selector table value for the branches must be updated in accordance with predicting which prediction strategy to go with in order to be effective, the same is true either way it is predicted).

In regard to claim 4, Patt taught all the limitations as previously described, however Patt did not explicitly state *wherein the circuitry for updating the selector table is further operable to maintain a value in a selected entry in the selector table when corresponding values from the bimodal and fetch based branch history tables both correctly represent a corresponding branch resolution*. However, considering the two prediction schemes have both predicted correctly, it would take more time and system resources to update the prediction selection scheme. This would be unnecessarily wasteful since both prediction schemes are equally accurate at this point. Therefore, it would have been an obvious implementation to one of ordinary skill in the art since there is no indication of why two values which are working should be changed.

In regard to claim 5, Patt taught all the limitations as previously described, however Patt did not explicitly state *wherein the circuitry for updating the selector table*

is further operable to maintain a value in a selected entry in the selector table when neither values from the bimodal and fetch based branch history tables both correctly represent a corresponding branch resolution. However, considering the two prediction schemes have both predicted incorrectly, it would take more time and system resources to update the prediction selection scheme. This would be unnecessarily wasteful since both prediction schemes are both wrong at this point. Therefore, it would have been an obvious implementation to one of ordinary skill in the art since there is no indication of why two values which are not working should be changed.

In regard to claim 6, Patt taught the previous limitations. However, Patt did not explicitly state the additional limitation *wherein the circuitry for updating the selector table is further operable to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome.* The fetched based table is using two level prediction scheme (page 253, item 4). The two level prediction is beneficial with better accuracy over other predictors (page 255, section 4.1, first two sentences). Clearly if two level prediction is a beneficial concept over other prediction schemes, it would have been an obvious implementation to one of ordinary skill in the art to record the fetch-based based table as the one the selector should choose, since it is likely to be more accurate.

In regard to claim 8, Patt taught the limitations as follows:

i) *a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits* (page 253, section 3.1, item 2 of the bulleted list)

ii) *a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits* (page 253, section 3.1, item 4; the fetch-based system is the two-level branch predictor)

iii) *a selector for selecting in response to a selection control mechanism selected from a set of selection control bits, a mechanism from a selected one of the sets of bits accessed from the first and second history tables* (page 255, section 4, first paragraph)

iv) *a selector table comprising a plurality of entries for storing the set of selector bits as a function of a performance history of the first and second sets of branch prediction bits stored in the first and second branch history tables* (page 255, section 4.1, first paragraph).

Patt did not explicitly state *the selector in response to a control bit* and for choosing *a control bit.* However, it is well known that a single bit is all that is required for the selection of two separate choices and in that since simplicity produces efficiency. Therefore, it would have been obvious to one of ordinary skill in the art to implement Patt with a single bit for selection purposes.

In regard to claim 9, Patt taught the limitation *wherein the entries of the selector table are accessed using fetch-based accessing* (page 255, section 4.1, first paragraph).

In regard to claim 11, Patt taught the limitation *wherein the first and second branch history tables and the selector table from a portion of a branch execution unit* (branch prediction is performed within branch execution units).

In regard to claim 12, Patt taught the limitation *wherein the branch execution unit forms a part of a microprocessor* (page 252, Abstract).

In regard to claim 13, Patt taught the limitation *and further comprising memory coupled to the microprocessor* (microprocessors include many different elements that are considered "memory", everything from registers, cache, stacks, even the tables for branch prediction; therefore, Patt has memory coupled to the microprocessor).

In regard to claim 14, Patt taught the limitations as follows:

i) *A method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table* (page 253, items 2 and 4; and page 255, section 4.1, first paragraph)

ii) *accessing the bimodal branch history table to retrieve a first branch prediction bit* (page 253, item 2; this is the operation of the predictor sited)

iii) *accessing the fetch-based branch history table to retrieve a second branch prediction bit* (page 253, item 4; this is the operation of the predictor sited)

iv) *selecting between the first and second branch prediction bits in response to a bit retrieved from the selector table* (page 252, section 2, first two sentences)

v) *updating the selector table as a function of actual branch resolution* (necessary in order have an effective two level selection predictor, page 255, section 4.1).

Though all of the above functionality is performed, Patt did not explicitly state the use of a single selection bit as written the above limitations. However, it is well known that a single bit is all that is required for the selection of two separate choices and in that since simplicity produces efficiency. Therefore, it would have been an obvious implementation to one of ordinary skill in the art for Patt to use a single bit for selection purposes.

In regard to claim 15, Patt taught the additional limitations as follows:

i) *determining if the first branch prediction bit correctly predicts the branch resolution outcome* (this must be included in Patt in order for the selector to be effective when it is updated)

ii) *updating the corresponding entry in the selector table to a first logic value when the first prediction bit correctly represents the branch resolution outcome* (this must be included if the prediction circuitry is to be able to accurately predict)

iii) *determining if the second branch prediction bit correctly predicts the branch resolution outcome* (this must be included in Patt in order for the selector to be effective when it is updated)

iv) *updating the corresponding entry in the selector table to a second logic value when the second branch prediction bit correctly represents the branch resolution outcome* (this must be included if the prediction circuitry is to be able to accurately predict)

In regard to claims 16 and 17, the limitations are essentially the same as the above claims 3-6, only relating to different base claims. However, the base claims and

all the limitations contained therein are rejected in a similar manner and therefore, the claims 16 and 17 and their limitations are rejected with a similar argument as claims 3-6.

In regard to claim 18, Patt taught the additional limitation *wherein the step of accessing the fetch-based history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register* (page 253, section 3.1, item 4).

6. Claims 7, 10, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al. "Alternative Implementations of Hybrid Branch Predictors", Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257 in view of Hennessy et al. Computer Architecture: A Quantitative Approach, Morgan Kaufmann Publishers, Inc.; pp. 269.

In regard to claim 7, Patt taught the preceding limitations of the base claims as noted above. Patt did not explicitly state the limitation *wherein the history register comprises circuitry for updating the shift register by shifting in a preselected value in response to a prediction value from a selected one of the branch history tables as selected in response to a corresponding selector bit.* This is found in Hennessy on page 269, second paragraph on the page. It clearly talks of a simplicity of design using the shift register. Therefore, since simplicity of design is always a great benefit which would help improve Patt, it would have been obvious to one of ordinary skill in the art to implement Patts history register as a shift register as found in Hennessy.

In regard to claim 10, Patt taught the preceding limitations of the base claims as noted above. Patt did not explicitly state the limitation *wherein each entry in the tables comprises a 1-bit counter*. This is found in Hennessy on page 269, in the second paragraph. Here n-bit predictors are discussed for a branch, this n could be a 1 and therefore 1-bit counter is mentioned as part of a simplicity of circuitry. Motivated by the advantage of simple circuitry which would improve Patt, it would have been obvious to one of ordinary skill in the art to implement Patt with counters as discussed be Hennessy.

In regard to claims 19 and 20, the limitations are essentially the same as for above claim 7, the only difference being the claims are related to different base claims. However, the base claims are rejected in a similar manner, and therefore the argument for rejection of claims 19 and 20 is similar to the rejection for claim 7.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

McFarling et al. (USPN 5,758,142) taught the concept of multiple prediction strategies being selected from a selector in order to improve the overall prediction

accuracy based on the strengths of the separate prediction strategies. This applicable to claims 1-20.

Baweja et al. (USPN 6,332,189) taught the concepts of branch prediction using local, bimodal, and global prediction strategies.

Patt et al., "Alternative Implementations of Two-Level Adaptive Branch Prediction", taught the concepts surrounding two-level prediction.

Chang et al., "Branch Prediction Using Both Global and Local Branch History Information", taught further concepts involving selection of two different prediction strategies to improve performance of branch prediction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
May 15, 2002

EDDIE CHAN
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